FIG. 1

DATA PROCESSOR 4

CPU

6   8   ~7   1   2

13
HISTORY INFORMATION STORAGE PART

14   22
23
26
24
25

10
11

15

DATA ARRAY
17

ADDRESS ARRAY
16

18
COMPA-RA-TOR

19A   12   30
19B   31

(WAY 0)
(WAY 1)

~43   42~   ~40   ~41

MEMORY CONTROL PART   ~3

DATA   ADDRESS   CONTROL INFORMATION

FIG. 2

FIG. 3

FIG. 4

```
        ┌─────────────┐
        │    START    │
        └──────┬──────┘
               │                     S1
    ┌──────────┴───────────┐
    │ PERFORM WAY PREDICTION│
    │  ACCORDING TO CACHE   │
    │   ACCESS HISTORY      │
    │   INFORMATION FOR     │
    │    CPU ADDRESS        │
    │ TO SUPPLY DATA TO CPU │
    └──────────┬───────────┘
               │                     S2
          ╱────┴────╲         NO
    ╱─────────────────────╲──────────┐
    ╲   ANY WAY IS HIT ?  ╱          │              S3
    ╲─────────┬─────────╱    ┌───────┴────────┐
              │ YES          │ PERFORM EXTERNAL│
              │              │  MEMORY ACCESS TO│
              │              │ SUPPLY DATA TO CPU│
              │              │    AND UPDATE    │
              │              │ PREDICTION HISTORY│
              │              └───────┬────────┘
          ╱───┴────╲   S4            │
NO   ╱───────────────────╲     ┌─────┴─────┐
┌────╲  PREDICTION MISS ? ╱     │    END    │
│    ╲─────────┬────────╱       └───────────┘
│              │ YES   S5      CACHE MISS
┌──┴──┐        │
│ END │   ┌────┴──────────────┐
└─────┘   │ PERFORM RE-READING OF│
CACHE HIT │ THE OTHER WAY TO SUPPLY│
PREDICTION│ DATA TO CPU AND UPDATE │
   HIT    │  PREDICTION HISTORY    │
          └────────┬──────────────┘
                   │
              ┌────┴────┐
              │   END   │
              └─────────┘
              CACHE HIT
              PREDICTION
                 MISS
```

START

S1
PERFORM WAY PREDICTION ACCORDING TO CACHE ACCESS HISTORY INFORMATION FOR CPU ADDRESS TO SUPPLY DATA TO CPU

S2
ANY WAY IS HIT ?

NO

S3
PERFORM EXTERNAL MEMORY ACCESS TO SUPPLY DATA TO CPU AND UPDATE PREDICTION HISTORY

END
CACHE MISS

YES

S4
PREDICTION MISS ?

NO

END
CACHE HIT PREDICTION HIT

YES

S5
PERFORM RE-READING OF THE OTHER WAY TO SUPPLY DATA TO CPU AND UPDATE PREDICTION HISTORY

END
CACHE HIT PREDICTION MISS

FIG. 5

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R3	R3	R4	R4	R4	R5	R5	R5	
ADDRESS ARRAY ACCESS	R1			R2			R3			R4			R5	
DATA ARRAY ACCESS	R1		R1	R2		R2	R3		R3	R4		R4	R5	
HISTORY INFORMATION PREDICTED WAY	W0		W1	W0		W1	W0		W1	W0		W1	W0	
WAY SELECT	W0		W1	W0		W1	W0		W1	W0		W1	W0	
LOCATION OF CPU REQUESTING DATA	W1 for R1			W1 for R2			W1 for R3			W1 for R4			W1 for R5	
CPU RECEIVING DATA	W0 for R1		W1 for R1	W0 for R2		W1 for R2	W0 for R3		W1 for R3	W0 for R4		W1 for R4	W0 for R5	
ACCESS STATE	R1 IS PRE-DICTION MISS			R2 IS PRE-DICTION MISS			R3 IS PRE-DICTION MISS			R4 IS PRE-DICTION MISS			R5 IS PRE-DICTION MISS	
EXTERNAL MEMORY ACCESS														

FIG. 6

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R4	R4	R4	R5					
ADDRESS ARRAY ACCESS	R1	(R2)		(R2)	R3	R4		(R4)	R5					
DATA ARRAY ACCESS	R1		R1	R2	R3		R3	R4	R5					
HISTORY INFORMATION PREDICTED WAY	W0	W0	W1	W0	W0	W0	W1	W0	W0					
WAY SELECT	W0		W1	W1	W0		W1	W1	W0					
LOCATION OF CPU REQUESTING DATA	W1 for R1			W1 for R2	W1 for R3			W1 for R4	W1 for R5					
CPU RECEIVING DATA	W0 for R1		W1 for R1	W1 for R2	W0 for R3		W1 for R3	W1 for R4	W0 for R5					
ACCESS STATE	R1 IS PRE-DICTION MISS			R2 IS PRE-DICTION HIT	R3 IS PRE-DICTION MISS			R4 IS PRE-DICTION HIT	R5 IS PRE-DICTION MISS					
EXTERNAL MEMORY ACCESS														
COMPLETION SIGNAL	1	0 ※	0	1	1	0	0 ※	1	1					

FIG. 7

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R2	R2	R3	R3	R3	R4	R4	R4	R4	R5
ADDRESS ARRAY ACCESS	R1					R2			R3					R4
DATA ARRAY ACCESS	R1					R2		R2	R3					R4
HISTORY INFORMATION PREDICTED WAY	W0					W0		W1	W0					W0
WAY SELECT	W0					W0		W1	W0					W0
LOCATION OF CPU REQUESTING DATA	EX-TERNAL MEMORY					W1 for R2			EX-TERNAL MEMORY					W1 for R2
CPU RECEIVING DATA	W0 for R1				Data for R1	W0 for R2		W1 for R2	W0 for R3				Data for R3	W0 for R4
ACCESS STATE	R1 IS CACHE MISS					R2 IS PRE-DICTION MISS			R3 IS CACHE MISS					R4 IS PRE-DICTION MISS
EXTERNAL MEMORY ACCESS		ISSUE R1								ISSUE R3				

FIG. 8

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R2	R2	R3	R4	R4	R4	R4	R4		
ADDRESS ARRAY ACCESS	R1	(R2)				(R2)	R3	R4				(R4)		
DATA ARRAY ACCESS	R1					R2	R3					R4		
HISTORY INFORMATION PREDICTED WAY	W0					W0	W0					W0		
WAY SELECT	W0					W1	W0					W1		
LOCATION OF CPU REQUESTING DATA	EXTERNAL MEMORY					W1 for R2	EXTERNAL MEMORY					W1 for R4		
CPU RECEIVING DATA	W0 for R1				Data for R1	W1 for R2	W0 for R3				Data for R1	W1 for R4		
ACCESS STATE	R1 IS CACHE MISS					R2 IS PREDICTION HIT	R3 IS CACHE MISS					R4 IS PREDICTION HIT		
EXTERNAL MEMORY ACCESS		ISSUE R1						ISSUE R3						
1 COMPLETION SIGNAL	1	0 ※	0	0	0	1	1	0 ※	0	0	0	1	1	

FIG. 9

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R3	R3	R3	R3	R4	R4	R4	R5	R5
ADDRESS ARRAY ACCESS	R1			R2					R3			R4		
DATA ARRAY ACCESS	R1		R1	R2					R3		R3	R4		
HISTORY INFORMATION PREDICTED WAY	W0		W1	W0					W0		W1	W0		
WAY SELECT	W0		W1	W0					W0		W1	W0		
LOCATION OF CPU REQUESTING DATA	W1 for R1			EX-TERNAL MEMORY					W1 for R3			EX-TERNAL MEMORY		
CPU RECEIVING DATA	W0 for R1		W1 for R1	W0 for R2				Data for R2	W0 for R3		W1 for R3	W0 for R4		
ACCESS STATE	R1 IS PRE-DICTION MISS			R2 IS CACHE MISS					R3 IS PRE-DICTION MISS			R4 IS CACHE MISS		
EXTERNAL MEMORY ACCESS					ISSUE R2								ISSUE R4	

FIG. 10

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R3	R3	R4	R4	R4	R5	R5	R5	
ADDRESS ARRAY ACCESS	R1	R2		R2			R3	R4		R4			R5	
DATA ARRAY ACCESS	R1		R1	R2			R3		R3	R4			R5	
HISTORY INFORMATION PREDICTED WAY	W0		W1	W0			W0		W1	W0				
WAY SELECT	W0		W1	W0			W0		W1	W0				
LOCATION OF CPU REQUESTING DATA	W1 for R1			EXTERNAL MEMORY			W1 for R3			EXTERNAL MEMORY				
CPU RECEIVING DATA	W0 for R1		W1 for R1	W0 for R1		Data for R2	W0 for R3		W1 for R1	W0 for R4		Data for R4		
ACCESS STATE	R1 IS PREDICTION MISS			R2 IS CACHE MISS			R3 IS PREDICTION MISS			R4 IS CACHE MISS				
EXTERNAL MEMORY ACCESS			ISSUE R2						ISSUE R4					
COMPLETION SIGNAL	1	0	0	1	0	0	1	0	0	1	0	0	1	

FIG. 11

4A

DATA PROCESSOR

CPU

6   8   7   1   2A

13A

HISTORY
INFORMATION
STORAGE
PART

22

15

24A   26

10

11

25

DATA
ARRAY

17

18

19A

ADDRESS
ARRAY

16

COMPA-
RA-
TOR

23

30

31A

19B

12A

(WAY 0)

(WAY 1)

43   42   40   41   3

MEMORY CONTROL PART

DATA   ADDRESS   CONTROL
INFORMATION

FIG. 12

INDEX ADDRESS
INFORMATION

FIG. 13

4B

DATA PROCESSOR

CPU

HISTORY INFORMATION STORAGE PART

SWITCHING REGISTER

DATA ARRAY

ADDRESS ARRAY

COMPA-RA-TOR

CACHE CONTROL PART

(WAY 0)
(WAY 1)

MEMORY CONTROL PART

DATA   ADDRESS   CONTROL INFORMATION